CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of operating a flash memory array comprising the steps of:

setting a counter to a first predetermined value each time a memory block associated with said counter is erased;

incrementing a counter respectively associated with another memory block in said flash memory array; and

refreshing the data in a memory block of said flash memory array when an associated counter equals or exceeds a predetermined threshold value.

2. A method as in claim 1, wherein said first predetermined value is zero.

3. A method as in claim 1, wherein said refreshing comprises storing data from a memory block to be erased in a different block in said flash memory array or in a different flash memory array.

4. A method as in claim 3, wherein said refreshing further comprises leaving said data in said different memory block when said refreshing is complete.

5. A method as in claim 1, wherein said refreshing comprises restoring said data from said memory block in said memory block.

6. A method as in claim 5, wherein said data is restored in the same locations in a memory block as it is read from.

7. A method as in claim 5, wherein refreshing further comprises optimizing the locations said data is stored in.

8. A method as in claim 1, wherein refreshing comprises dividing said data into pieces, each of said pieces being refreshed after a distinct, unrelated operation is completed by said flash memory array.

9. A method as in claim 8, wherein each of said pieces is refreshed after a write command is executed by said flash memory array.

10. A method as in claim 1, wherein the values of said counters are stored in a table.

11. A method as in claim 10, wherein said table is stored in said flash memory array.

12. A method as in claim 10, wherein said table is stored in a table in a separate memory storage device.

13. A method as in claim 10, wherein the most significant byte and the second most significant byte of each entry in said table are set to predetermined binary values.

14. A method as in claim 13, wherein said predetermined binary values are 11111111 and 11110110.

15. A method as in claim 10, wherein the entries of said table contain N data bytes, each bit of an entry corresponding to one memory block of N based on said bit's position within said entry.

16. A method as in claim 10, wherein entries in said table contain eight data bytes.

17. A method of operating a flash memory array comprising the steps of:

erasing a memory block;

setting a counter associated with said memory block to a first predetermined value;

incrementing counters respectively associated with all other memory blocks in the same main block;

refreshing all memory blocks that have associated counters which equal or exceed a second predetermined value.

18. A method of operating a flash memory array comprising the steps of:

erasing a memory block;

setting the counter associated with said memory block to a first predetermined value;

decrementing the counters associated with all other memory blocks within the same main block;

refreshing all memory blocks that have associated counters which equal or exceed a second predetermined value.

19. A method as in claim 17 or 18, wherein said first predetermined value is zero.

20. A method as in claim 17 or 18, wherein said refreshing comprises storing data from a memory block in a different block in said flash memory array.

21. A method as in claim 17 or 18, wherein said data is restored in the same locations it is read from.

22. A method as in claim 17 or 18, wherein said refreshing comprises dividing said data into pieces, each of said pieces being refreshed after a distinct, unrelated operation is completed by said flash memory array.

23. A method as in claim 22, wherein each of said pieces is refreshed after a write command is executed by said flash memory array.

24. A method of operating a flash memory array comprising the steps of:

setting a counter to a first predetermined value each time a sector of a memory block associated with said counter is programmed;

incrementing a counter respectively associated with each adjacent sector of said memory block in said flash memory array; and

refreshing the data in a sector of a memory block of said flash memory array when an associated counter equals or exceeds a predetermined threshold value.

25. A method as in claim 24, wherein said first predetermined value is zero.

26. A method as in claim 24, wherein said refreshing comprises storing data from a sector of a memory block to be erased in a different sector in said flash memory array.

27. A method as in claim 27, wherein said refreshing further comprises leaving said data in said different sector when said refreshing is complete.

28. A method as in claim 24, wherein said refreshing comprises restoring said data from said sector.

29. A method as in claim 28, wherein said data is restored in the same locations in a sector as it is read from.

30. A method as in claim 28, wherein refreshing further comprises optimizing the locations said data is stored in.

31. A method as in claim 24, wherein when the counters associated with multiple sectors equal or exceed said predetermined threshold simultaneously, said refreshing comprises refreshing each sector after a distinct, unrelated operation is completed by said flash memory array.

32. A method as in claim 31, wherein each of said sectors is refreshed after a write command is executed by said flash memory array.

33. A method as in claim 24, wherein the values of said counters are stored in a table.

34. A method as in claim 33, wherein said table is stored in said flash memory array.

35. A method as in claim 33, wherein said table is stored in a table in a separate memory storage device.

36. A method as in claim 33, wherein the most significant byte and the second most significant byte of each entry in said table are set to predetermined binary values.

37. A method as in claim 36, wherein said predetermined binary values are 11111111 and 11110110.

38. A method as in claim 33, wherein the entries of said table contain N data bytes, each bit of an entry corresponding to one memory block of N based on said bit's position within said entry.

39. A method as in claim 33, wherein entries in said table contain eight data bytes.

40. A method of operating a flash memory array comprising the steps of:

programming a sector in a memory block;

setting a counter associated with said sector to a first predetermined value;

incrementing counters respectively associated with all other sectors adjacent to said programmed sector;

refreshing all sectors that have associated counters which equal or exceed a second predetermined value.

41. A method of operating a flash memory array comprising the steps of:

programming a sector in a memory block;

setting a counter associated with said sector to a first predetermined value;

decrementing counters respectively associated with all other sectors adjacent to said programmed sector;

refreshing all sectors that have associated counters which equal or exceed a second predetermined value.

42. A method as in claim 40 or 41, wherein said first predetermined value is zero.

43. A method as in claim 40 or 41, wherein said refreshing comprises storing data from a sector in a different sector in said flash memory array.

44. A method as in claim 40 or 41, wherein said data is restored in the same locations it is read from.

45. A method as in claim 40 or 41, wherein when the counter associated with multiple sectors equal or exceed said second predetermined value simultaneously, said refreshing comprises refreshing each of said sectors after a distinct, unrelated operation is completed by said flash memory array.

46. A method as in claim 45, wherein each of said pieces is refreshed after a write command is executed by said flash memory array.

47. A flash memory storage device comprising:

a control circuit; and

a data storage area divided into a plurality of memory blocks for storing data and a table for storing a plurality of counters;

wherein when said control circuit erases data stored in one of said memory blocks, said control circuit sets the counter associated with said erased memory block to a first predetermined value and increments counters respectively associated with other memory blocks; and

wherein when one of said plurality of counters equals or exceeds a predetermined threshold value, said control circuit refreshes the data in the memory block associated with said counter.

48. A flash memory device as in claim 47, wherein said control circuit refreshes said memory block associated with a counter that equals or exceeds said predetermined threshold value by storing the data stored in said memory block in a different memory block.

49. A flash memory storage device as in claim 47, wherein said control circuit refreshes said memory block associated with a counter that equals or exceeds said predetermined threshold value by storing the data stored in said memory block in said memory block.

50. A flash memory storage device as in claim 49, wherein said control circuit restores said data to the same locations in said erased memory block.

51. A flash memory storage device as in claim 47, wherein said control circuit optimizes said data prior to restoring said data.

52. A flash memory storage device as in claim 47, wherein when a counter associated with a memory block equals or exceeds said predetermined threshold value , said control circuit divides said data into pieces, said control circuit refreshing each of said pieces after performing a distinct, unrelated operation.

53. A flash memory storage device as in claim 52, wherein said control circuit refreshes each of said pieces after performing a write command.

54. A flash memory storage device as in claim 47, wherein the values of said counters are stored in a table.

55. A flash memory storage device as in claim 54, wherein said table is stored in said flash memory storage device.

56. A flash memory storage device as in claim 54, wherein said table is stored in a separate memory storage device.

57. A flash memory storage device as in claim 54, wherein the most significant byte and the second most significant byte of each entry in said table are set to predetermined binary values.

58. A flash memory storage device as in claim 57, wherein said predetermined binary values are 11111111 and 11110110 respectively.

59. A flash memory storage device as in claim 54, wherein the entries in said table are N bytes, each bit of an entry corresponding to one of N memory blocks based on said bit's position within said entry.

60. A flash memory storage device comprising:

a control circuit; and

a data storage area divided into a plurality of memory blocks, said memory blocks further divided into a plurality of sectors, for storing data and a table for storing a plurality of counters;

wherein when said control circuit programs one of said sectors, said control circuit sets the counter associated with said programmed sector to a first predetermined value and increments counters respectively associated with all sectors adjacent to said programmed sector; and

wherein when one of said plurality of counters equals or exceeds a predetermined threshold value, said control circuit refreshes the data in the sector associated with said counter.

61. A flash memory storage device as in claim 60, wherein said control circuit refreshes said sector associated with a counter that equals or exceeds said predetermined threshold value by storing the data stored in said sector in a different sector.

62. A flash memory storage device as in claim 60, wherein said control circuit refreshes said sector associated with a counter that equals or exceeds said predetermined threshold value by storing the data stored in said sector in said sector.

63. A flash memory storage device as in claim 62, wherein said control circuit restores said data to the same locations in said sector.

64. A flash memory storage device as in claim 61 or 62, wherein said control circuit optimizes said data prior to restoring said data.

65. A flash memory storage device as in claim 60, wherein when counters associated with multiple sectors equals or exceed said predetermined threshold value simultaneously, said control circuit refreshes each of said sectors after performing a distinct, unrelated operation.

66. A flash memory storage device as in claim 65, wherein said control circuit refreshes each of said sectors after performing a write command.

67. A flash memory storage device as in claim 60, wherein the values of said counters are stored in a table.

68. A flash memory storage device as in claim 67, wherein said table is stored in said flash memory storage device.

69. A flash memory storage device as in claim 67, wherein said table is stored in a separate memory storage device.

70. A flash memory storage device as in claim 67, wherein the most significant byte and the second most significant byte of each entry in said table are set to predetermined binary values.

71. A flash memory storage device as in claim 70, wherein said predetermined binary values are 11111111 and 11110110 respectively.

72. A flash memory storage device as in claim 67, wherein the entries in said table are N bytes, each bit of an entry corresponding to one of N memory blocks based on said bit's position within said entry.

73. A processor circuit comprising:

a processor; and

a flash memory storage device coupled to said processor, said flash memory storage device comprising a plurality of memory storage regions and a plurality of counters, each of said plurality of counters associated with one of said plurality of memory storage regions;

wherein when data stored in one of said memory storage regions is erased, the counter associated with said memory storage region is set to a first predetermined value and the remaining counters are incremented; and

wherein when one of said plurality of counters equals or exceeds a predetermined threshold value, the data in the memory storage region associated with said counter is refreshed.

74. A processor circuit as in claim 73, wherein said first predetermined value is zero.

75. A processor circuit as in claim 73, wherein said flash memory storage device refreshes said memory storage region associated with a counter that equals or exceeds said predetermined threshold value by storing the data stored in said memory block in a different memory block.

76. A processor circuit as in claim 73, wherein said flash memory storage device restores said data to the same locations in said erased memory block.

77. A processor circuit as in claim 73, wherein when a memory storage region requires refreshing, said flash memory storage device divides said memory storage region into pieces, said flash memory storage device refreshing each of said pieces after a distinct, unrelated operation is completed by said flash memory storage device.

78. A processor circuit as in claim 77, wherein said flash memory storage device refreshes each of said pieces after a write commands are executed by said flash memory storage device.

79. A processor circuit as in claim 73, wherein the values of said counters are stored in a table.

80. A processor circuit as in claim 79, wherein said table is stored in said flash memory storage device.

81. A processor circuit as in claim 79, wherein said table is stored in a separate memory storage device.

82. A processor circuit as in claim 79, wherein the entries in said table comprise N bytes each, each bit of each entry corresponding to one memory block of N based on said bit's position within said byte.

83. A processor circuit as in claim 79, wherein the most significant byte and the second most significant byte of each table entry are set to a predetermined binary values.

84. A processor circuit as in claim 83, wherein said predetermined binary values are 11111111 and 11110110 respectively.

85. A processor circuit comprising:

a processor; and

a flash memory storage device coupled to said processor, said flash memory storage device comprising a plurality of memory storage regions, said memory storage regions being divided into a plurality of sectors, and a plurality of counters, each of said plurality of counters associated with one of said sectors;

wherein when one of said sectors is programmed, the counter associated with said sector is set to a first predetermined value and all of the sectors adjacent to said programmed sector incremented; and

wherein when one of said plurality of counters equals or exceeds a predetermined threshold value, the data in the sector associated with said counter is refreshed.

86. A processor circuit as in claim 85, wherein said first predetermined value is zero.

87. A processor circuit as in claim 85, wherein said flash memory storage device refreshes said sector associated with a counter that equals or exceeds said predetermined threshold value by storing the data stored in said sector in a different sector.

88. A processor circuit as in claim 85, wherein said flash memory storage device restores said data to the same in said sector.

89. A processor circuit as in claim 85, wherein when the counters associated with multiple sectors equal or exceed said predetermined value simultaneously, said flash memory storage device refreshes each of said sectors after a distinct, unrelated operation is completed by said flash memory storage device.

90. A processor circuit as in claim 89, wherein said flash memory storage device refreshes each of said sectors after a write commands are executed by said flash memory storage device.

91. A processor circuit as in claim 85, wherein the values of said counters are stored in a table.

92. A processor circuit as in claim 91, wherein said table is stored in said flash memory storage device.

93. A processor circuit as in claim 91, wherein said table is stored in a separate memory storage device.

94. A processor circuit as in claim 91, wherein the entries in said table comprise N bytes each, each bit of each entry corresponding to one memory block of N based on said bit's position within said byte.

95. A processor circuit as in claim 91, wherein the most significant byte and the second most significant byte of each table entry are set to a predetermined binary values.

96. A processor circuit as in claim 95, wherein said predetermined binary values are 11111111 and 11110110 respectively.